

## BIO DATA



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Designation : Assistant Professor (Sr.Gr.)

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Google Scholar link:

<https://scholar.google.com/citations?user=BxxBP7gAAAAJ&hl=en>

### 1. Educational Qualification

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Degree	Branch / Specialization	Institute/University	Year of Passing
B.E.	ECE	S.Veerassamy Chettiar College of Engineering and Technology / Anna University	2007
M.E	VLSI Design	Government College of Technology, Coimbatore / Anna University	2011
Ph.D	VLSI Design	Anna University	Synopsis Submitted

### 2. Professional/ Industry Experience

: (in chronological order)

S.No	Designation	Institution/ Organization	Period	
			From	To
1	Assistant Professor (SG) / ECE	Ramco Institute of Technology	03.12.2014	Till date
2	Assistant Professor / ECE	S.Veerassamy Chettiar College of Engineering and Technology	15.9.2014	19.11.2014
3	Assistant Professor / ECE	Kalasalingam University	01.07.2011	05.11.2012
4	Teaching Fellow & Research Scholar	Government College of Technology	07.01.2013	12.9.2014
5	Lecturer / ECE	Lakshmi Ammal Polytechnic College	02.05.2008	04.05.2009

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6	System Analyst	M.S Graphics and Designing	01.06.2007	30.04.2008
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### 3. Research Interest: VLSI Design and Image Processing

#### 4 Publications

##### 4.1 JOURNAL PUBLICATIONS

1. **Azhagu Jaisudhan Pazhani A, Vasanthanayaki C** (2019), "Design and Implementation of Computationally Efficient Arithmetic Unit", Journal of Electrical Engineering, Vol.No.19 PP-228-237
2. **Azhagu Jaisudhan Pazhani A, Vasanthanayaki C** (2014), " Design of Multi Output Binary Adder using Modified Parallel Prefix Addition", Advances in Natural and Applied Sciences, Vol.No.8, PP 10-16
3. **Azhagu Jaisudhan Pazhani A, Vasanthanayaki C** (2015), " FPGA Implementation of Computationally Efficient Modified Parallel Prefix Adder", Advances in Natural and Applied Sciences , Vol.No.10, PP 367-371
4. **Azhagu Jaisudhan Pazhani A, Renisha.V, Veeralakshmi.R, Vinitha.R, 2017**, "FPGA Implementation of Fast Multiplier using Interlaced Partition Concept" SSRG International Journal of Electronics and Communication Engineering.
5. **Azhagu Jaisudhan Pazhani A, Abirami A, Iashikha S V, Taj din Irfana J, 2017**, "FPGA Implementation of Reconfigurable Error Tolerant Carry Look Ahead Adder (RET-CLA)"SSRG International Journal of Electronics and Communication Engineering

##### 4.2 CONFERENCE PUBLICATIONS

1. **Azhagu Jaisudhan Pazhani.A, Akshaya Gomathi C, Joanna Karen W, Karpagavalli M and Meena L** (2019), "Design of Low power and Area Efficient Computation Unit using Memorization Concept", National Conference on Computer Science and Applications (NCCSA 2019), Ramco Institute of Technology
2. **Azhagu Jaisudhan Pazhani.A, Gyathri.N, Muthu Janani M G, and Naveena B**, "Design of Area Efficient Approximate ACT Architecture for Image Compression", National Conference on Computer Science and Applications (NCCSA 2019), Ramco Institute of Technology
3. **Azhagu Jaisudhan Pazhani.A, Logeswari.M, Mahalakshmi.P and Muthumeena.B** (2019), "An Area Efficient VLSI Architecture for Binary Division", National Conference on Innovations in Communication Technology for Social Development (ICTSD 2018), Ramco Institute of Technology.
4. **Azhagu Jaisudhan Pazhani.A, Pushpavalli S, Rasmica T S, Sivaranjani S** (2018), "VLSI Computational Architectures for the Arithmetic Cosine Transform", National Conference on Innovations in Communication Technology for Social Development (ICTSD 2018), Ramco Institute of Technology.
5. **Azhagu Jaisudhan Pazhani.A, Sangeetha.M, Sashi Sri Jeyam R and Suruthi K** (2018), "High speed Error Tolerant Multiplier using Rounding Based Approximation" , International Conference on Engineering and Advancement in Technology, Sri Krishna College of Technology

### 4.3 Book/Book chapter publications

**Author(s) Initial(s). Title of the Book, xth ed. Publisher, Year of Publication, pp. xxx–xxx.**

### 5 Funded Projects

S.No.	Title of the project	Funding Agency	Duration	Amount	Status
1	Low Power and area efficient DCT algorithm for image processing application (2018)	FAER – McAfee Scholar Programme	6 Months	5000	Completed
2	Low Power and area efficient DCT algorithm for image processing application (2019)	FAER – McAfee Scholar Programme	6 Months	5000	Completed

### 6 Ph.D. guidance

Sl.No	Scholar name	University	Topic	Status

### 7 Short term Courses / Seminars /FDP/Workshop/ConferenceAttended:

Sl.No	Title f the event	Organized by	Date	
			From	To
1.	AU sponsored FDTP on “EC6502 – Principles of Digital Signal Processing”	Department of ECE, Ramco Institute of Technology	03.06.2015	10.06.2015
2.	Training Programme on “NI LabVIEW Core 1 & Core 2 course	Ramco Institute of Technology in association with National Instruments	15.06.2015	19.06.2015
3.	Faculty development training program on VLSI Design	National Engineering college, Kovilpatti	01.12.2015	08.12.2015
4.	Awareness & Internal Auditor Training on ISO 9001:2015	TUVRheinland	18.12.2015	19.12.2015
5.	Workshop on “Embedded Systems and its Applications”	Department of ECE, Ramco Institute of Technology	21.12.2015	22.12.2015
6.	Value Added Course on “VLSI Design Simulation”	Department of ECE, Ramco Institute of Technology	14.12.2015	17.12.2015
7.	Value Added Course on “Project Based Learning using Arduino”	Department of ECE, Ramco Institute of Technology	09.12.2015	13.12.2015
8.	FDP on “Train the Trainers”	Ramco Institute of Technology	22.06.2015	23.06.2015

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9.	FDP on “Research Methodologies”	Ramco Institute of Technology	18.11.2016	19.11.2016
10.	Tenth National Seminar on Research Issues in Digital Image Processing	Mepco Schlenk Engineering College	18.03.2017	
11.	FDTP on “ RF and Microwave Engineering”	Department of ECE, Ramco Institute of Technology	12.06.2017	16.07.2017
12.	AICTE sponsored FDTP on “Human Values and Professional Ethics”	Department of EEE, Ramco Institute of Technology	30.10.2017	12.11.2017
13.	Electronic System Design and Manufacturing (ESDM) & Testing Using CADENCE OrCAD & OrCAD PCB & MITS PCB Prototyping Solutions	Entuple Technologies Pvt. Ltd	27.11.2017	01.12.2017
14.	Train the Trainers	Tessolve Semiconductor Limited	20.11.2017	24.11.2017
15.	FDTP on “Signals and systems”	Department of ECE, Ramco Institute of Technology	13.06.2018	18.06.2018
16.	Two Day Workshop on “Writing Research Papers, Citation Analysis, Plagiarism, Getting Patent & Copyright”	Department of Library, Ramco Institute of Technology	29.06.2018	30.06.2018
17.	Art of Counseling	Ramco Institute of Technology	19.06.2018	21.06.2018
18.	ISO Awareness & Internal Auditing Training for ISO 9001:2015	Ramco Institute of Technology in association with TUV Rheinhold(India) Pvt.Ltd	21.06.2018	22.06.2018
19.	One day Orientation and Awareness Program on OBE and SAR preparation	Ramco Institute of Technology	23.11.2019	
20.	Advanced RF Circuit Design and Software Defined Radio	Government College of Engineering, Salem	12.06.2019	25.06.2019

**8. Short term Courses / Seminars /FDP/Workshop/Conference organized:**

Sl.No	Title of the event	Organized by	Date	
			From	To
1.	TECHYUGA '2K19 State Level Technical Symposium	Ramco Institute of Technology	31.08.2019	-
2.	Value Added Course – Tessolve Semiconductor IC Testing	Ramco Institute of Technology	13.06.2018	18.06.2018

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3.	Second National Conference on Innovations in Engineering ,Science and Technology	Department of ECE, Ramco Institute of Technology	23.03.2018	
4.	National Science day	Ramco Institute of Technology	28.02.2018	
5.	Engineers Day Celebration 2018	Department of ECE, Ramco Institute of Technology	15.09.2018	
6.	Tech yuga – Paper Presentation	Ramco Institute of Technology	31.08.2018	
7.	National Science day – Technical Quiz	Ramco Institute of Technology	28.02.2017	
8.	First National Conference on Innovations in Engineering ,Science and Technology	Ramco Institute of Technology	24.03.2017	
9.	Guest Lecture on Internet of things	Ramco Institute of Technology	13.04.2017	
10.	Tech yuga – Report Preparation and feedback Committee	Ramco Institute of Technology	28.08.2017	
11.	National Science day – Mini project Coordinator	Ramco Institute of Technology	28.02.2016	
12.	Value added course on VLSI Design using Cadence Tool	Ramco Institute of Technology	14.12.2015	18.12.2015

### 9. Online Courses

Sl. No.	Course title	University	Date
1.	Circuits and Electronics 1: Basic Circuit Analysis	MIT	14.05.2016
2.	Electronic Materials and Devices	MIT	01.07.2016
3.	Circuits and Electronics 2: Amplification, Speed, and Delay	MIT	05.05.2017
4.	Calculus 1A: Differentiation	MIT	15.09.2017
5.	Calculus 1B: Integration	MIT	09.03.2018
6.	Differential Equations: Fourier Series and Partial Differential Equations	MIT	21.12.2018
7.	Calculus 1C: Coordinate Systems & Infinite Series	MIT	12.05.2019
8.	Circuits and Electronics 3: Applications	MIT	04.06.2019

### 10. Patents filed/awarded: Nil

### 11. Membership in Professional societies: ISTE

### 12. Awards, Recognition & Achievements

- Internal ISO 9001:2015 audit.
- Achieved 100% results in university examination
- Got Certificate of Merit in FAER McAfee Scholar Program 2018.

**Any others (Board of studies/Governing Council/Staff Selection/ Reviewer/other duties)**

<b>Sl.No.</b>	<b>Position held</b>	<b>Period</b>	<b>Activities carried out</b>
1	Department Placement Coordinator	2016 – Till now	<ul style="list-style-type: none"> <li>• Prepare, maintaining and updating the students data regarding placement, Made the necessary arrangement and also accompanied with the students for attending online aptitude test, helping the students for registered in particular websites and online courses, guiding and motivating the students for preparation in Quantitative aptitude, puzzles and technical aptitude .</li> <li>• Addressing the student about the company profile</li> </ul>
2	E-Cell Coordinator	2016 – Till now	<ul style="list-style-type: none"> <li>• Guiding and motivating the students to attend the workshop/ seminar regarding entrepreneurship development</li> </ul>
3	VLSI Design Lab Incharge	2015 –Till now	<ul style="list-style-type: none"> <li>• Laboratory Time Table preparation, Laboratory Manual Preparation, updating and maintaining the laboratory stock registers, monitoring laboratory cleanliness, purchase order preparation</li> </ul>
4	Tessolve Semiconductor IC Testing Trainer	2019-2020	<ul style="list-style-type: none"> <li>• Provide industry related training to students during evening time and making the students to get opportunity in TESSOLVE SEMICODUCTOR</li> </ul>
5	NBA - Criteria 3	2019 - 2020	<ul style="list-style-type: none"> <li>• Department Coordinator – Collecting all the data related to Criteria 3</li> </ul>
6	ISO Internal Auditor	2019-2020	<ul style="list-style-type: none"> <li>• Auditing various departments at regular intervals</li> </ul>
7	Value Added Course Incharge For IC Testing	2019- 2020	<ul style="list-style-type: none"> <li>• Preparing syllabus, time table and providing laboratory training to the students.</li> </ul>
8	NAAC – Criteria 2 Department Incharge	2019 -2020	<ul style="list-style-type: none"> <li>• Collecting Department Data’s for NAAC Criteria 2</li> </ul>
9	Class Committee Chairperson	2019-2020	<ul style="list-style-type: none"> <li>• Committee meetings were conducted at regular intervals and monitoring the students’ progress, performance and discipline</li> </ul>