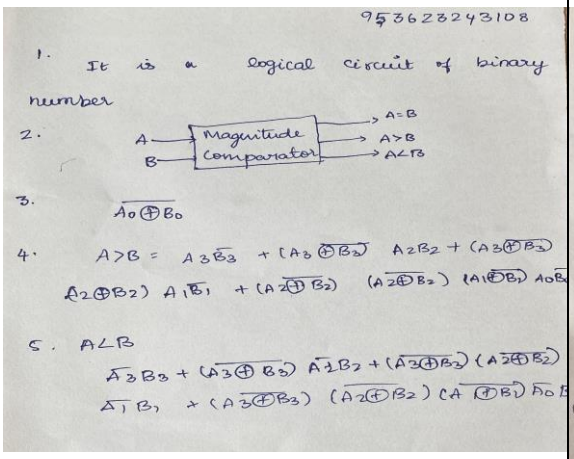
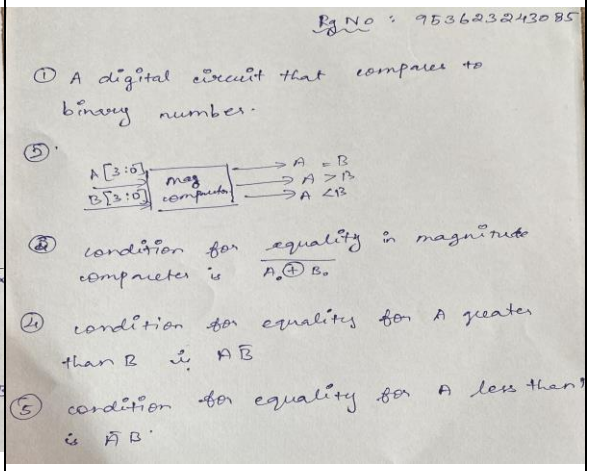
Department of Electronics and Communication Engineering
Academic Year 2024 – 2025 (Odd Semester)

Innovative Teaching Method

UNIT I – Combinational Logic

Degree, Semester & Branch: B.Tech., III Semester & AI & DS B
Course Code & Title: CS3351 & Digital Principles and Computer Organization
Name of Faculty member : Ms.L.Krishna Kumari
Name of the Topic: Magnitude Comparator
Name of the Innovative Practice: One-minute Speech
Date & Duration:10.08.2024 & 5 minutes
Sample Images:

Innovative Teaching Method Execution	
Magnitude Comparator	
	
	

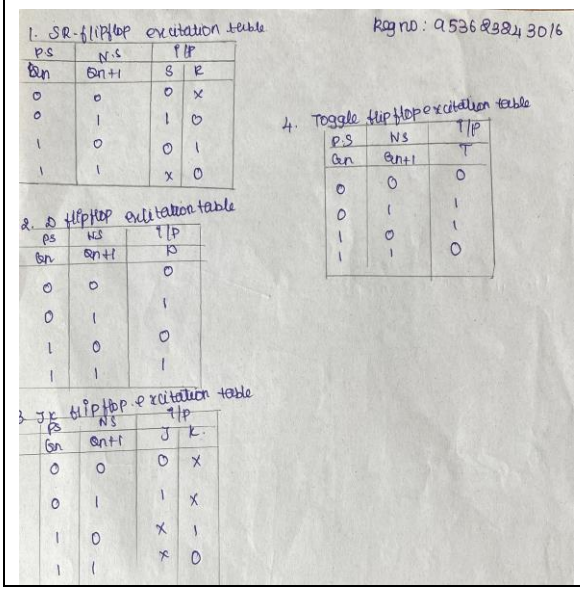
Department of Electronics and Communication Engineering
Academic Year 2024 – 2025 (Odd Semester)

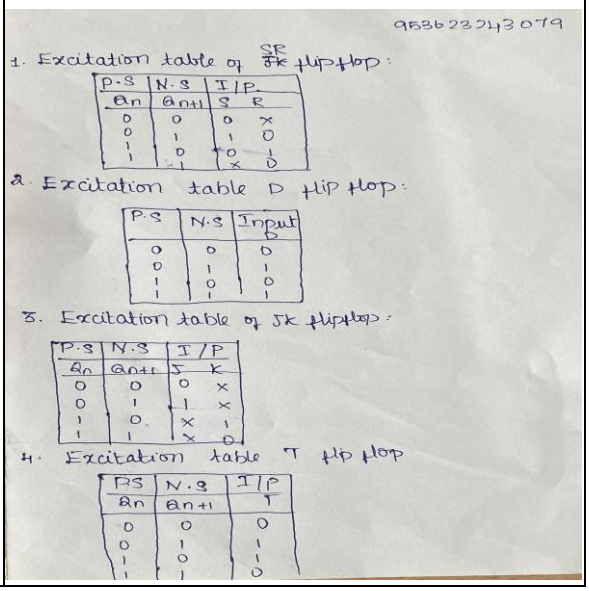
Innovative Teaching Method

UNIT II – Synchronous Sequential Logic

Degree, Semester & Branch: B.Tech., III Semester & AI & DS B
Course Code & Title: CS3351 & Digital Principles and Computer Organization
Name of Faculty member : Ms.L.Krishna Kumari
Name of the Topic: Flip Flops Operation, Excitation Table
Name of the Innovative Practice: Mind Map
Date & Duration: 19.08.2024 & 5 minutes
Sample Images:

Innovative Teaching Method Execution
Flip Flops Operation, Excitation Table

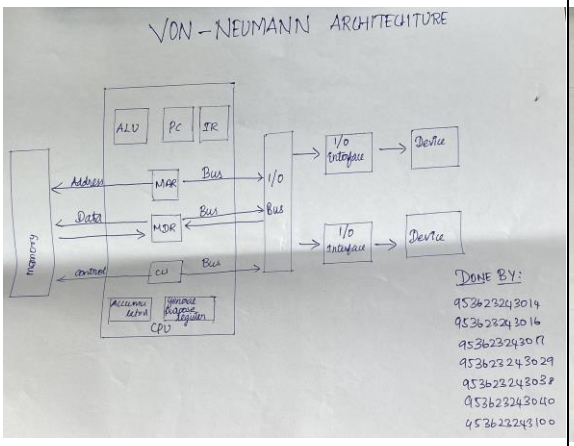
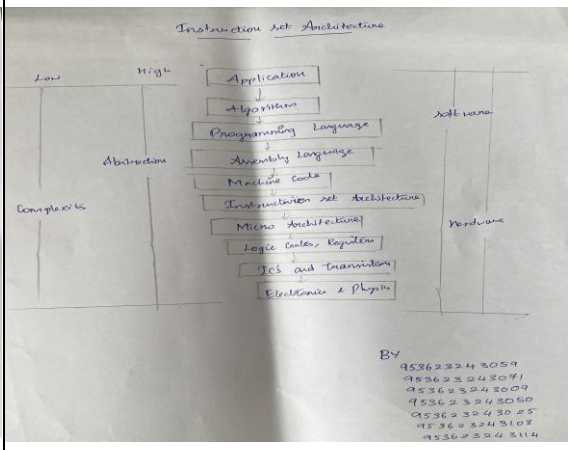




Department of Electronics and Communication Engineering
Academic Year 2024 – 2025 (Odd Semester)
Innovative Teaching Method

UNIT III – Computer Fundamentals

Degree, Semester & Branch: B.Tech., III Semester & AI & DS B
Course Code & Title: CS3351 & Digital Principles and Computer Organization
Name of Faculty member : Ms.L.Krishna Kumari
Name of the Topic: Von Neumann Architecture & ISA Architecture
Name of the Innovative Practice: Write Pair Share
Date & Duration: 09.09.2024 & 15 minutes
Sample Images:

Innovative Teaching Method Execution	
Von Neumann Architecture & ISA Architecture	
	
	

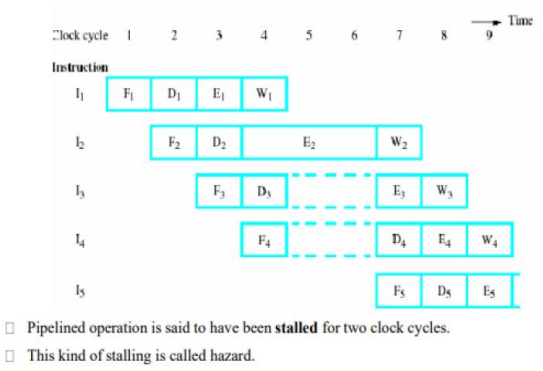
Department of Electronics and Communication Engineering
Academic Year 2024 – 2025 (Odd Semester)

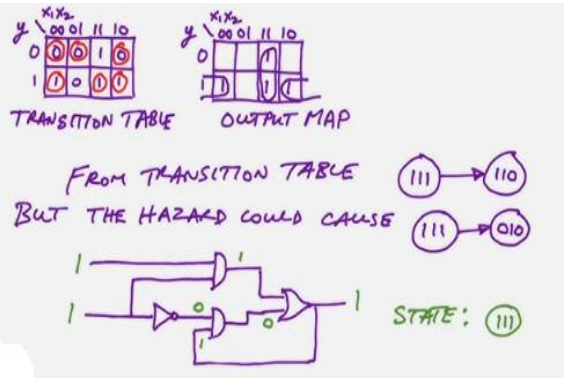
Innovative Teaching Method

UNIT IV– Processor

Degree, Semester & Branch: B.Tech., III Semester & AI & DS B
Course Code & Title: CS3351 & Digital Principles and Computer Organization
Name of Faculty member : Ms.L.Krishna Kumari
Name of the Topic: Hazards in digital circuits
Name of the Innovative Practice: Exit Slips and Animation
Date & Duration: 23.10.2024 & 15 minutes
Sample Images:

Innovative Teaching Method Execution
Von Neumann Architecture & ISA Architecture





Department of Electronics and Communication Engineering
Academic Year 2024 – 2025 (Odd Semester)
Degree, Semester & Branch: B.Tech., III Semester & AI & DS B
Course Code & Title: CS3351 & Digital Principles and Computer Organization
Name of Faculty member : Ms.L.Krishna Kumari

Innovative Practice Description

- **Unit / Topic:** V/ Memory and I/O - Cache Memories
- **Course Outcome:** CO5
- **Topic Learning Outcome:** 5.3
- **Activity Chosen:** Flipped Class room
- **Justification:**

The topic chosen for flipped class is cache memories, Unit 5 deals with Memory and I/O covers concepts like memory management, cache memories, I/O and Interconnection standards. This topic can be learnt in self-learning mode with simple manipulations, Mapping concepts and logics. The students have the chance to browse the topic to know how the cache memories were mapped and its schematic representations. Thus this flipped class activity is chosen to make them to work out different mapping techniques of cache memories.

- **Time Allotted for the Activity:** 45 minutes
- **Details of the Implementation:**

The overview of flipped class activity was given to students before the implementation of the activity. The students were divided into groups and one topic is allotted to each group from cache memories topic as their wish. The topic related information and e-sources were given to the students. The students have to prepare a presentation for 10 minutes and each group has to present their topic chosen and others will listen to the presentation. After the presentation, question & answering is planned and others can share their ideas and doubts. By this way, all groups were shared their concepts learnt in their topic inside the class.

- **CO – PO / PSO mapping:**

CO	PO1	PO2	PO8	PO9	PO10	PO12	PSO1	PSO2	PSO3
CO5	3	3	2	2	2	2	1	2	1

- **PO / PSO mapped**

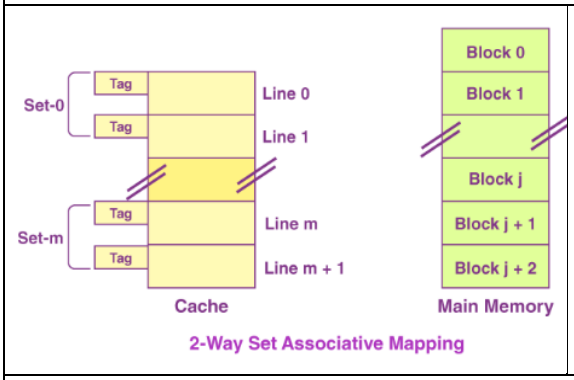
Innovative practice	PO2	PSO2
	3	2

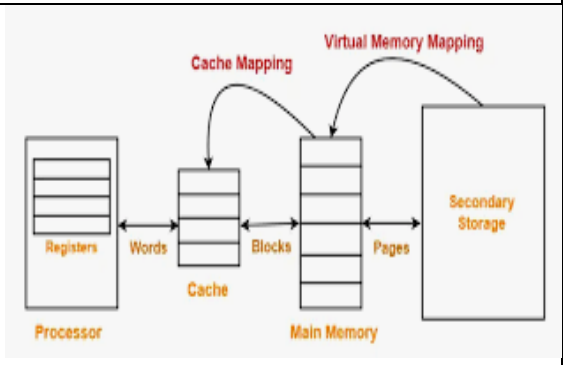
Justification for correlation	The outcome is mapped to level 3 by identifying the mathematical and engineering knowledge needed to solve problems in the memory chip organization.	The students will be able to solve existing problems in parallel bus architectures. Hence, it is mapped at level 2.

- **Images / Screenshot of the practice:**

Innovative Teaching Method Execution

Cache memories





- **Reflective Critique:**
  - ❖ ***Feedback of practice from students and other stakeholders:***

    The students felt a new practice and it helped them to know to make good presentation and avoid stage fear. They liked this practice of teaching that can be done through this type of activity. They could get idea from learning sources which would help them to prepare the presentation.

  - ❖ ***Benefit of the practice:***

    Students done this activity in a successful manner. They planned the activity for their chosen topic and prepared the presentation in the conceptual manner. All members in the group were learnt the topics thoroughly. By forming the group, students were able to grasp the knowledge of concept by sharing the ideas among them. Each member in the group was able to present and deliver the concept of Buck, boost, buck boos analysis and design.

- ***Challenges faced in implementation:***

  Some of the students felt difficult to present because of lack of communication. Few groups done their presentation beyond their time limit. Few students in the group felt difficult to answer all the questions.

References:

1. M. Morris Mano, Michael D. Ciletti, "Digital Design : With an Introduction to the Verilog HDL, VHDL, and System Verilog", Sixth Edition, Pearson Education, 2018.

2. David A. Patterson, John L. Hennessy, "Computer Organization and Design, The Hardware/Software Interface", Sixth Edition, Morgan Kaufmann/Elsevier, 2020.