



# RAMCO INSTITUTE OF TECHNOLOGY

Approved by AICTE, New Delhi & Affiliated to Anna University  
Accredited by NAAC & An ISO 9001:2015 Certified Institution  
NBA Accredited UG Programs: CSE, EEE, ECE and MECH

## Department of Electronics and Communication Engineering

Academic Year 2024 – 2025 (Odd Semester)

Degree, Semester & Branch: V Semester B.E & ECE A

Course Code & Title: EC3552 & VLSI and Chip

### Innovative Practice Description

- **Unit / Topic:** V/ ASIC Design Flow, Introduction to ASICs
- **Course Outcome:** CO5
- **Activity Chosen:** Flipped Class room
- **Justification:**
  - The flipped classroom approach is ideal for teaching ASIC Design Flow and Introduction to ASICs as it allows students to independently explore the multi-step process of designing application-specific integrated circuits before class. By engaging with pre-class resources such as videos and readings, students can familiarize themselves with key concepts like RTL design, synthesis, verification, and physical design at their own pace. In-class time is then used for hands-on activities, problem-solving, and collaborative learning, where students can apply their knowledge through practical exercises using industry-standard tools, discuss design trade-offs, and work on real-world challenges. This active learning environment promotes deeper understanding, critical thinking, and prepares students for the complex and interdisciplinary nature of ASIC design, ensuring they are better equipped for industry applications.
- **Time Allotted for the Activity:** 45 minutes
- **Details of the Implementation:**

The overview of flipped class activity was given to students before the implementation of the activity. The students were divided into groups and one topic is allotted to each group from cache memories topic as their wish. The topic related information and e-sources were given to the students. The students have to prepare a presentation for 10 minutes and each group has to present their topic chosen and others will listen to the presentation. After the presentation, question & answering is planned and others can share their ideas and doubts. By this way, all groups were shared their concepts learnt in their topic inside the class.
- **CO – PO / PSO mapping:**

CO	PO1	PO2	PO4	PO9	PO10	PO12	PSO3
CO5	3	3	2	1	1	1	3

• **PO / PSO mapped**

Innovative practice	PO4	PSO3
	2	3
<b>Justification for correlation</b>	It is mapped to level 2 because since the students will determine design objectives, functional requirements and arrive at specifications of the ASIC design flow	to In the field of communication systems, students will be able to understand the concepts of ASIC Hence it is mapped at level 3.

• **Images / Screenshot of the practice:**



• **Reflective Critique:**

❖ ***Feedback of practice from students and other stakeholders:***

The students felt a new practice and it helped them to know to make good presentation and avoid stage fear. They liked this practice of teaching that can be done through this type of activity. They could get idea from learning sources which would help them to prepare the presentation.

❖ ***Benefit of the practice:***

Students done this activity in a successful manner. They planned the activity for their chosen topic and prepared the presentation in the conceptual manner. All members in the group were learnt the topics thoroughly. By forming the group, students were able to grasp the knowledge of concept by sharing the ideas among them. Each member in the group was able to present and deliver the concept.

❖ ***Challenges faced in implementation:***

Some of the students felt difficult to present because of lack of communication.  
Few groups done their presentation beyond their time limit.  
Few students in the group felt difficult to answer all the questions.

**References:**


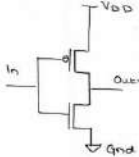
- 1 D.A. Hodges and H.G. Jackson, Analysis and Design of Digital Integrated Circuits, International Student Edition, McGraw Hill 1983
2. P. Rashinkar, Paterson and L. Singh, “System-on-a-Chip Verification-Methodology and Techniques”, Kluwer Academic Publishers,2001
3. SamihaMourad and YervantZorian, “Principles of Testing Electronic Systems”, Wiley 2000
4. M. Bushnell and V. D. Agarwal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers,2000



Department of Electronics and Communication Engineering  
Academic Year: 2024 – 2025(ODD Semester)

## INNOVATIVE TEACHING METHODS

Degree, Semester & Branch : V Semester B.E & ECE  
Course Code & Title : EC3552 & VLSI and Chip Design  
Name of the Faculty member: Mrs.G.Subhashini, AP/ECE


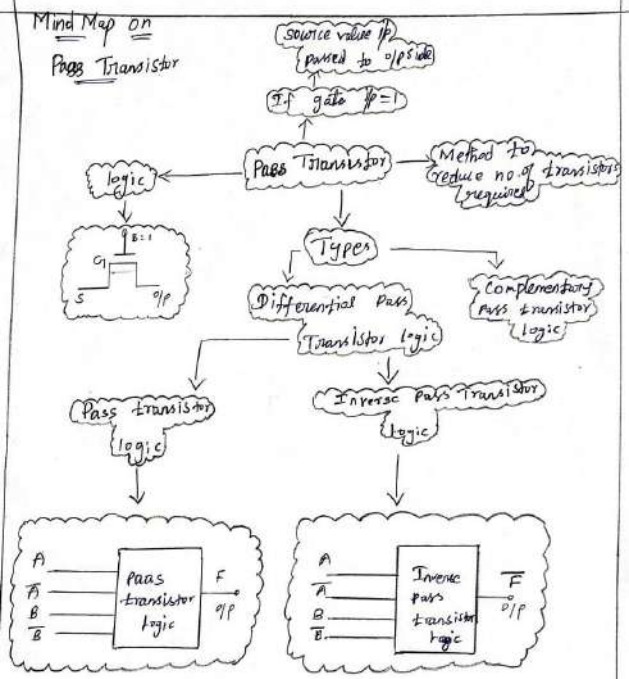
Sl.No.	Date	Topic(s)	Activity*	Reference
<b>UNIT I-MOS Transistor Principles</b>				
1	12.08.2024	CMOS Devices	One minute paper	<a href="https://oncourseworkshop.com/self-awareness/one-minute-paper/">https://oncourseworkshop.com/self-awareness/one-minute-paper/</a>
			<p>CMOS: 95362210609)</p> <p>It is abbreviated as Complementary Metal - oxide semiconductor</p> <p>The combination of NMOS &amp; PMOS</p> <p>Inverter Diagram Using CMOS:</p>  <p>When the I/P is high the pmos will be in off condition therefore there is no connection b/w VDD &amp; out but the NMOS will be ON therefore the out is grounded therefore the o/p will be low</p> <p>When the I/P is low the pmos will be in on condition therefore the output will be high.</p>	



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Sl.No.	Date	Topic(s)	Activity*	Reference
<b>UNIT II-COMBINATIONAL LOGIC CIRCUITS</b>				
1.	30.08.2024	Pass Transistor Logic	Mind Map	<a href="https://www.nasa.gov/sites/default/files/files/4-TWPS_Template.pdf">https://www.nasa.gov/sites/default/files/files/4-TWPS_Template.pdf</a>
			 <p style="text-align: right;">By: 953622106093 ECE-'B'</p>	



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Sl.No.	Date	Topic(s)	Activity*	Reference
<b>UNIT III</b> <b>SEQUENTIAL LOGIC CIRCUITS AND CLOCKING STRATEGIES</b>				
1.	23.09.2024	Timing Classification of Digital System	Head and Talk	





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Sl.No.	Date	Topic(s)	Activity*	Reference
<b>UNIT IV</b> <b>INTERCONNECT , MEMORY ARCHITECTURE AND ARITHMETIC CIRCUITS</b>				
1.	22.10.2024	Logic Implementation using Programmable Devices (ROM, PLA, FPGA)	Jigsaw	
