Department of Electronics and Communication Engineering
Academic Year 2024 – 2025 (Odd Semester)
Degree, Semester & Branch: III Semester B.Tech. CS&BS
Course Code & Title: CS3351 & Digital Principles and Computer Organization

Innovative Practice Description

- **Unit / Topic:** V/ Cache Memories
- **Course Outcome:** CO5
- **Activity Chosen:** Flipped Class room
- **Justification:**
- Cache memory is an essential topic in computer architecture that enhances system performance by bridging the speed gap between the CPU and main memory. This topic covers cache mapping techniques (direct, associative, and set-associative), replacement policies, and performance metrics like hit and miss rates. A flipped classroom approach is ideal because students can independently explore these concepts using available resources. Self-learning allows them to understand how data is stored and retrieved efficiently, analyze the impact of different mapping techniques, and visualize cache operations through diagrams. Students can also experiment with numerical examples, such as calculating cache hit rates, which reinforce their analytical skills. During in-class activities, discussions can focus on problem-solving, comparing mapping techniques, and analyzing trade-offs in cache design. This approach promotes active learning, critical thinking, and collaborative problem-solving, making the topic both engaging and impactful.
- **Time Allotted for the Activity:** 45 minutes
- **Details of the Implementation:**

  The overview of flipped class activity was given to students before the implementation of the activity. The students were divided into groups and one topic is allotted to each group from cache memories topic as their wish. The topic related information and e-sources were given to the students. The students have to prepare a presentation for 10 minutes and each group has to present their topic chosen and others will listen to the presentation. After the presentation, question & answering is planned and others can share their ideas and doubts. By this way, all groups were shared their concepts learnt in their topic inside the class.

- **CO – PO / PSO mapping:**

CO	PO1	PO2	PO8	PO9	PO10	PO12	PSO1	PSO2	PSO 3
CO5	3	3	2	2	2	2	2	2	2

- **PO / PSO mapped**

Innovative practice	**PO3**	**PSO3**
	2	2
Justification for correlation	It is mapped to level 2 because since the students will determine design objectives, functional requirements and arrive at specifications of the cache memories	to In the field of communication systems, students will be able to understand the concepts of cache memories. Hence it is mapped at level 2.

- **Images / Screenshot of the practice:**

Innovative Teaching Method Execution	
Cache Memories	
	

- **Reflective Critique:**
  - ***Feedback of practice from students and other stakeholders:***
    The students felt a new practice and it helped them to know to make good presentation and avoid stage fear. They liked this practice of teaching that can be done through this type of activity. They could get idea from learning sources which would help them to prepare the presentation.
  - ***Benefit of the practice:***
    Students done this activity in a successful manner. They planned the activity for their chosen topic and prepared the presentation in the conceptual manner. All

members in the group were learnt the topics thoroughly. By forming the group, students were able to grasp the knowledge of concept by sharing the ideas among them. Each member in the group was able to present and deliver the concepts.

- ***Challenges faced in implementation:***

  Some of the students felt difficult to present because of lack of communication.
  Few groups done their presentation beyond their time limit.
  Few students in the group felt difficult to answer all the questions.

References:

1 Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Naraig Manjikian, "Computer Organization and Embedded Systems", Sixth Edition, Tata McGraw-Hill, 2012.

2. William Stallings, "Computer Organization and Architecture – Designing for Performance", Tenth Edition, Pearson Education, 2016.

3. M. Morris Mano, "Digital Logic and Computer Design", Pearson Education, 2016

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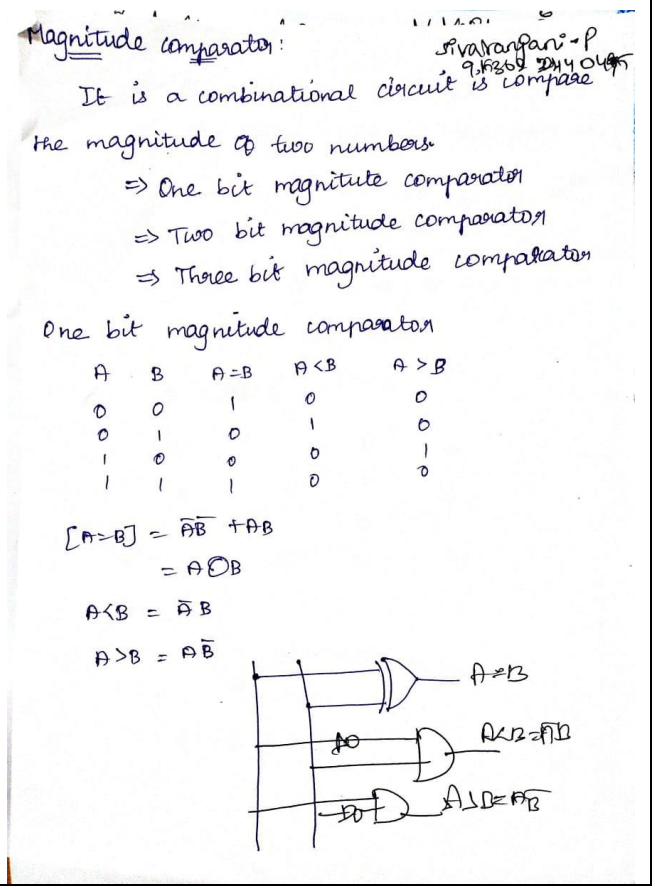
INNOVATIVE TEACHING METHODS

Degree, Semester & Branch : III Semester B.Tech. CS&BS
Course Code & Title : CS3351 & Digital Principles and Computer Organization
Name of the Faculty member: Mrs.G.Subhashini, AP/ECE

Sl.No.	Date	Topic(s)	Activity*	Reference
UNIT I- Combinational Logic				
1	10.08.2024	Magnitude Comparator	One minute paper	https://oncourseworkshop.com/self-awareness/one-minute-paper/



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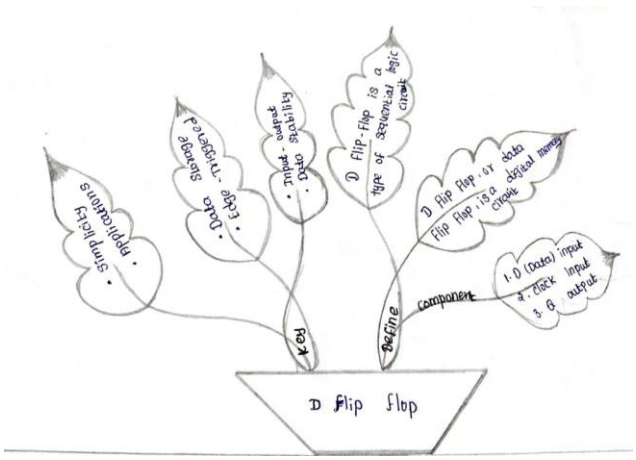
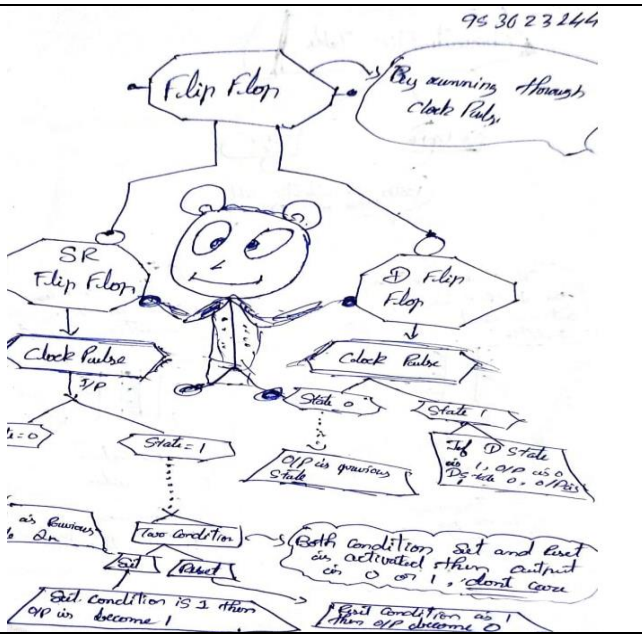
UNIT II- Synchronous Sequential Logic				
1	19.08.2024	Flipflop operation and Excitation Table	**Mind Map**	**https://www.figma.com/resource-library/mind-map-examples/**





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Sl.No.	Date	Topic(s)	Activity*	Reference
Unit-III Computer Fundamentals				
1	09.09.2024	Von Neumann Architecture & Operations and Operands	Write Pair Share	https://oncourseworkshop.com/self-awareness/one-minute-paper/